GF22: LVDS

AUTOMOTIVE GRADE

Libraries

Name	Process	Form Factor
RGO_GF22_18V25_FDX_UC_LVDS	FDX	Staggered CUP

Summary

The LVDS library provides an LVDS driver, receiver, and temperature stable voltage reference capable of supporting 16 drivers operating at data rates up to 3.6 Gbps. Also included is a full complement of power, spacer, and adapter cells to assemble a complete pad ring by abutment. An included rail splitter allows isolated LVDS domains to be placed in the same pad ring with other power domains while maintaining continuous VDD/VSS in the pad ring for robust ESD protection.

This 22nm library is available in a staggered CUP wire bond implementation with a flip chip option. The included adapter allows this library to used with Aragio inline GPIO libraries.

LVDS Specification Compliant:

- TIA/EIA-644-A - Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits
- IEEE Std 1596.3-1996

ESD Protection:

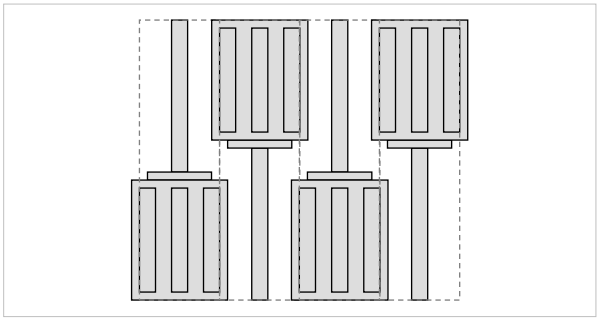
- JEDEC compliant
  - 2KV ESD Human Body Model (HBM)
  - 500 V ESD Charge Device Model (CDM)
    - 750V corner pin C4B package classification achieved by following key design priorities

Latch-up Immunity:

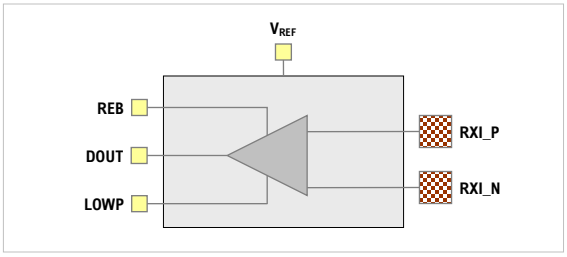
- JEDEC compliant
  - Tested to I-Test criteria of ± 100mA @ 125°C

Cell Size & Form Factor

Staggered (pad-limited) – 66μm x 79μm



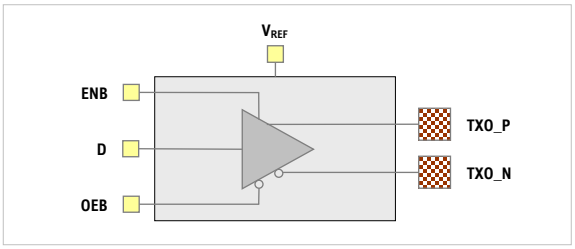
LDP_IN_800_25V_DN: 1.8GHz LVDS Receiver



LVDS Receiver Features:

- Operates up to 1.8 GHz (3.6 Gbps)
- Low power mode operates up to 1.2 GHz (2.4 Gbps) at half power
- Input receive sensitivity of 75mV peak differential (without hysteresis)
- Duty Cycle Distortion (DCD) – 50 ps typical
- Common mode range from 0V to 1.8V (limited by power supply)

LDP_OU_800_18V_T: 1.0GHz LVDS Driver



LVDS Driver Features:

- Operates up to 1.0 GHz (2.0 Gbps) with external 1 pF load
- Common mode output range 1.1V ±100mV
- Supports single termination (far end) only – 100Ω differential

GF22: LVDS

Recommended operating conditions

Symbol	Description	Min	Nom	Max	Units
V_{VDD}	Core supply voltage	0.81	0.9	0.945	V
		0.72	0.8	0.88	V
		0.59	0.65	0.715	V
		0.45	0.5	0.55	V
V_{DVDD}	I/O supply voltage	1.62	1.8	1.98	V
T_J	Junction temperature	-40	25	150	°C
V_{PAD}	Voltage at PAD	-0.3V		V_{DVDD}+0.3V	V
V_{IH}	Input high at PAD	0.7 * V_{DVDD}		V_{DVDD} + 0.3	V
V_{IL}	Input low at PAD	V_{DVSS} - 0.3		0.3 * V_{DVDD}	V

Characterization Corners

Nominal VDD	Model	VDD	DVDD[1]	Temperature
0.65V (AG2)	FFG	+10%	+10%	-40°C
	FFG	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SSG	0.59V	-10%	-40°C
	SSG	0.59V	-10%	125°C
0.8V / 0.5V (AG2)	FFG	+10%	+10%	-40°C
	FFG	+10%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SSG	-10%	-10%	-40°C
	SSG	-10%	-10%	125°C
0.9V Overdrive (AG2)	FFG	+5%	+10%	-40°C
	FFG	+5%	+10%	125°C
	TT	nominal	nominal	25°C
	TT	nominal	nominal	85°C
	SSG	-10%	-10%	-40°C
	SSG	-10%	-10%	125°C
0.8V (AG1)	FFG	+5%	+10%	-40°C
	FFG	+5%	+10%	125°C
	FFG	+5%	+10%	150°C
	SSG	-10%	-10%	150°C

[1] DVDD = 1.8V

Cell Summary & Physical Sizes

Name	Description
LDP_IN_800_25V_DN *	1.2 GHz LVDS input cell
LDP_OU_800_18V_T *	1.0 GHz LVDS output cell
LDP_RE_000_18V *	LVDS Voltage Reference cell
PVP_VD_RCD_10V *	Core power (VDD)
PVP_VS_RCD_10V *	Core ground (VSS)
PVP_VD_PDO_18V *	I/O power (DVDD) with POC control
PVP_VD_RDO_18V *	I/O power (DVDD)
PVP_VS_RDO_18V *	I/O ground (VSS)
SVP_SP_000_18V	0.1 µm spacer
SVP_SP_001_18V	1 µm spacer
SVP_SP_005_18V	5 µm spacer
SVP_SP_010_18V	10 µm spacer
SPP_RS_005_18V	Rail splitter
SPC_SPP_AD_UN	Staggered to inline adapter

*Supplied in vertical-only and horizontal-only orientations

Staggered CUP Cells	
CUP_GF22_44X44_IN	44µm X 44µm Inner
CUP_GF22_44X44_OUT	44µm X 44µm Outer
CUP_GF22_FC	Flip chip cell

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